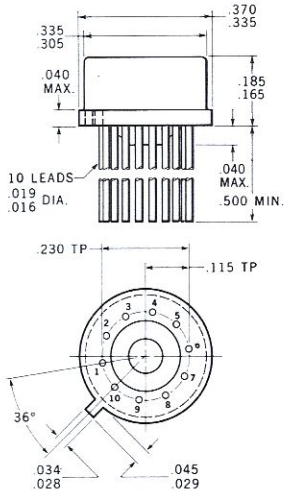
3303
MOS DUAL 25 BIT DYNAMIC SHIFT REGISTER
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3303 is a Dual 25 Bit Dynamic Shift Register. It is a monolithic integrated circuit utilizing Planar* II, P-Channel enhancement mode MOS technology. A two phase clock is used to reduce power consumption and increase speed.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Clock Voltages ($V_{\phi 1} = V_{\phi 2}$)	−30 V to +0.3 V
Data Input Voltage (V_{in})	−30 V to +0.3 V
Supply Voltage	−30 V to +0.3 V
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C

PHYSICAL DIMENSIONS
(In accordance with JEDEC TO−100)



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

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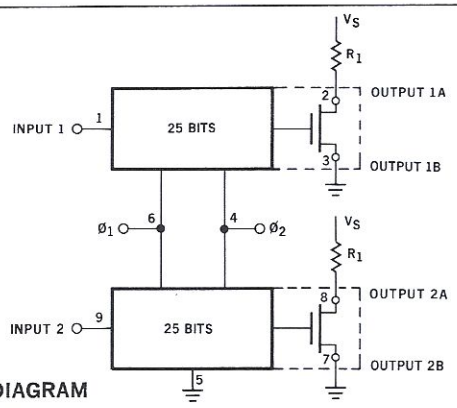
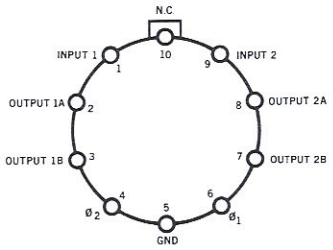


LOGIC DIAGRAM

The output device requires an external resistor (R_1), ground and power supply (V_S) and can be used either as an inverter or source follower (inverter shown).

CONNECTION DIAGRAM



TOP VIEW

NOTE:
(1) These ratings are limiting values above which the serviceability of the device may be impaired.

Electrical Characteristics on Page 2

*Planar is a patented Fairchild process.

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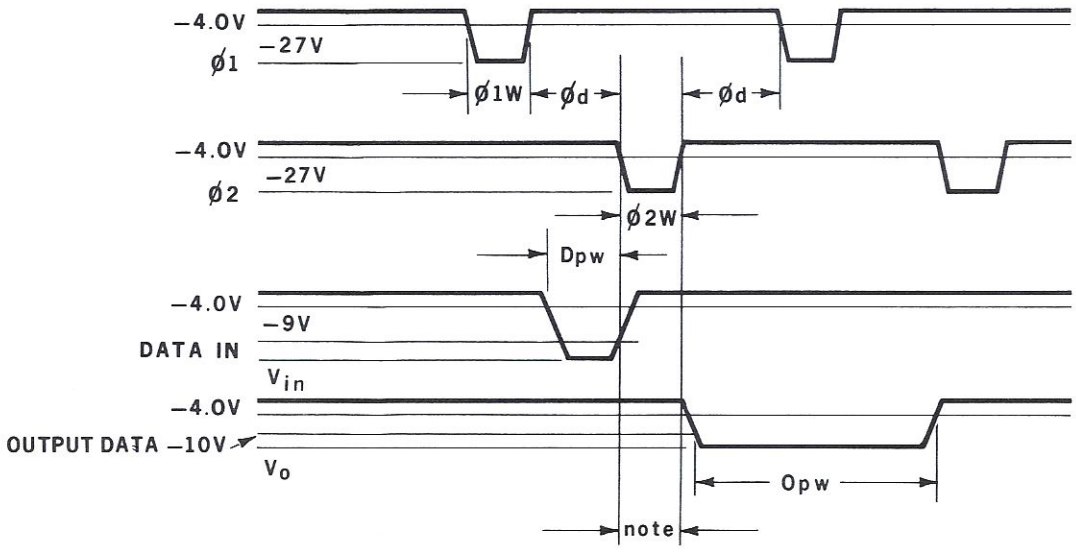
FAIRCHILD MOS INTEGRATED CIRCUIT 3303

ELECTRICAL CHARACTERISTICS

STANDARD CONDITIONS (unless otherwise specified)
Load . . . 10 MΩ and 10 pF
$V_S = -15\ V \pm 1.0\ V, V\phi = -27\ V \pm 1.0\ V$
$R_l = 20\ k\Omega$, $T_A = -55°C$ to $+85°C$

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
ϕ_1, ϕ_2	Clock Repetition Rate	10		500	kHz	
ϕ_{1w}, ϕ_{2w}	Clock Pulse Width	0.4		45	μs	
ϕ_d	Clock Delay	0.4			μs	
$V\phi$	Clock Pulse Amplitude					
	"0" Level	0		−0.5	Volts	
	"1" Level	−26		−28	Volts	
	Clock Pulse Rise and Fall Time (10% - 90%)			100	ns	
V_{in}	Data Input Logic Levels					
	Logic "0"	0		−2.0	Volts	
	Logic "1"	−9.0			Volts	$\phi_1 = 0.4\ \mu s$
D_{pw}	Data Pulse Width	200			ns	$\phi_2 = 0.4\ \mu s$
V_o	Output Logic Levels					
	Logic "0"			−1.0	Volts	
	Logic "1"	−10			Volts	
	Output Fall Time			550	ns	
O_{pw}	Output Pulse Width	1.0			μs	
R_o	Output Impedance to Ground			1000	Ω	
I_{CL}	Clock Input Leakage Current			100	μA	$V\phi = -26\ V$
	Data Input Capacitance		4.0		pF	$V\phi = 0\ V$
	Clock Input Capacitance		20		pF	$V\phi = 0\ V$
	Fan In			1.0		
	Fan Out			5.0		

TYPICAL WAVEFORMS



Note: Delayed 50 Bit Times